

masking, 62–63
 nonmaskable, 62
 return-from instruction, 62
 sharing memory, 93–94
 source and priority, 62
 UART, 100
 vector, 62, 123, 136, 142

Intersil, 346

inversion, *see* compliment, logical

IP (Internet Protocol), 194–195

ISA (Industry Standard Architecture) bus, 71

ISR (interrupt service routine)
 defined, 62
 serial communications, 66–67

ITU (International Telecommunication Union), 210

J

JEDEC (Joint Electron Device Engineering Council),
 78–79

joule, *see* energy

JTAG (Joint Test Action Group), 431–433
 BSDL (boundary scan description language), 433
 signals, 432

JTAG Technologies, 433

jumbo frame, *see* Ethernet

junction temperature, 378–379

K

Karnaugh map (K-map), 8–10

kernel, of OS, 139–140, 158–160

L

Lambda, 390

LSI (large-scale integration), 39

laser, 198

last-in-first-out, *see* stack

latch
 address, in 8051, 126–127
 avoidance in HDL, 229
 creation in HDL, 229–230
 defined, 21
 in SRAM, 86

Lattice Semiconductor, 252, 254, 255, 258

lead frame, 39

LSB (least-significant bit), 12

LED, *see* diode

LFSR (linear feedback shift register), 200, 209–210

linear regulator, *see* voltage regulator

Linear Technology, 107, 384, 388, 417

little-endian, 137, 212

locality
 caching, 150–151
 virtual memory, 160

logic
 7400 family, 42
 graphical representation, 6
 symbolic representation, 5–6

logic analyzer, 430–431, 442

logic cell, *see* FPGA

logic probe, 441

logic synthesis, 223–224, 226, 232

lookup table, 188
 FPGA, 257–258

loop analysis, 268–270

M

MAC, *see* Ethernet

macrocell, *see* PLD

magnetic
 crosstalk and EMI, 408–412
 inductor, 276

magnitude
 binary, 13
 frequency, 24
 time, 24

mantissa, floating-point, 165

mask
 instruction, 133
 interrupt, 62–63, 232
 photolithography, 36

Maxim, 106, 384, 388, 417

memory
 aliasing, 65
 architectural planning, 92
 bandwidth and RISC microprocessor, 148–149
 burst transactions to cache, 156
 bus expansion, 70–71
 cache, 150
 CAM, 189–191
 CS*, *see* chip select
 diagnostic testing, 433–434
 DMA, 68–69
 DRAM, 88–92
 dynamic, 78
 EEPROM, 85–86
 EPROM, 79
 FIFO, 94–96
 flash, 81–85

- general structure, 78
 - in a computer, 56
 - JEDEC standards, 78–79
 - location relative to cache, 150
 - lookup table, 188
 - microprocessor performance gap, 149
 - multiport, 92–94
 - OE*, *see* output enable
 - PROM, 79
 - protection in multitasking environment, 158–159
 - SDRAM, 173–179
 - SRAM, 86–88
 - SSRAM, 182–185
 - static, 78
 - system performance, 170–171
 - types, 77–78
 - WE*, *see* write enable
 - Mentor Graphics, 409, 436
 - mesh network topology, 110
 - metal
 - chassis, 413
 - deposition, 36
 - layers of an IC, 36
 - PCB, 393
 - metastability, *see* flip-flop
 - Microchip Technology, 86, 131, 149
 - microcontroller, 88, 119, 122, 232
 - 8051 and 8048, 125–126
 - PIC, 131–134
 - Micron Technology, 176, 183
 - micron, unit of measure, 35
 - microprocessor
 - 6800, 122–125
 - 68000, 139–142, 146–147
 - 8086, 134–138
 - addressing modes, 73–75
 - bandwidth improved by cache, 155
 - basic composition, 58–59, 61
 - bus, 57
 - bus expansion, 70–72, 229
 - bus fault, 141
 - bus FSM design example, 239, 241–242
 - bus interface design example, 227–229
 - cache, 150
 - CISC and RISC, 145–149
 - clock distribution design example, 361, 363
 - core clock synthesis, 364
 - debugging, 430
 - DSP, 167–169
 - Harvard architecture, 149
 - in a computer, 56
 - instruction prefetch, 164
 - interface to EPROM, 80–81
 - memory performance gap, 149
 - memory read, 65–66
 - memory write, 66–67, 90
 - performance metric, 169–170
 - pipelining, 162–163
 - reset circuit, 428–429
 - shared memory, 93–94
 - superscalar, 163–164
 - support logic, 227
 - MIPS microprocessor, 148
 - MMU (memory management unit), 158–161
 - mnemonic, 72
 - Model Technology, 224
 - modem, 104, 108–109
 - modulation, 108–109
 - Moore’s Law, 39
 - MOS (metal oxide semiconductor), 37, 306
 - MOSFET, *see* transistor
 - Motorola, 119, 122–125, 139, 146–147, 167
 - 6800 assembly language, 73–75
 - MPLS (multiprotocol label switching), 217
 - MSB (most-significant bit), 12
 - MSI (medium-scale integration), 39
 - multi
 - multicast address, 112
 - multiplexer
 - defined, 28
 - register read logic, 230–231
 - creating a FIFO with, 94–95
 - defined, 93
 - multitasking, 139
 - mutual inductance, *see* transformer
- N**
- National Semiconductor, 107, 346, 384, 388
 - negative number, *see* two’s compliment
 - netlist, 436
 - HDL synthesis, 223
 - PLD, 254, 256
 - schematic capture, 436
 - network
 - access sharing, 111–112
 - addressing, 111–112
 - arbitration, 112
 - collision detection, 113